ABSTRACT

A T-RAM array having a planar cell structure is presented. The T-RAM array includes n-MOS and p-MOS support devices which are fabricated by sharing process implant steps with T-RAM cells of the T-RAM array. A method is also presented for fabricating the T-RAM array having the planar cell structure. The method entails simultaneously fabricating a first portion of a T-RAM cell and the n-MOS support device; simultaneously fabricating a second portion of the T-RAM cell and the p-MOS support device; and finishing the fabrication of the T-RAM cell by interconnecting the T-RAM cell with the p-MOS and n-MOS support devices. The first portion of the T-RAM cell is a transfer gate and the second portion of the T-RAM cell is a gated-lateral thyristor storage element. Accordingly, process steps in fabricating the T-RAM cells are shared with process steps in fabricating the n-MOS and p-MOS support devices. The n-MOS and p-MOS support devices refer to sense amplifiers, wordline drivers, column and row decoders, etc. which are connected to the T-RAM array.